WHAT IS CLAIMED IS:

1. An integrated circuit (IC) package, comprising:

a first substrate;

a second substrate; and

a stiffener, wherein a surface of said first substrate is attached to a first surface of said stiffener, and a surface of said second substrate is attached to a second surface of said stiffener.

2. The package of claim 1, wherein a second surface of said second substrate has a central region that allows the attachment of an IC die.

3. The package of claim 1, wherein said second substrate has a centrally located opening configured to allow an IC die to attach to said second surface of said stiffener through said centrally located opening.

4. The package of claim 3, wherein said second surface of said stiffener is plated with a centrally located metal die-attach pad for attachment of said IC die.

5. The package of claim 1, wherein said first substrate includes at least one via through said first substrate.

6. The package of claim 5, wherein said at least one via is located in a central region of said first substrate.

7. The package of claim 6, wherein said first substrate has a second surface;

wherein said second surface of said first substrate includes a plurality of solder ball pads; and

wherein said at least one via couples said stiffener through said first substrate to at least one of said plurality of solder ball pads.

8. The package of claim 7, further comprising a conductive material in said at least one via.

9. The package of claim 1, wherein said first substrate has a centrally located opening, wherein said package further comprises:

a thermal connector that has a first surface coupled to said first surface of said stiffener through said centrally located opening, wherein a second surface of said thermal connector is configured to be coupled to a printed circuit board (PCB).

10. The package of claim 1, wherein said second substrate has at least one opening that exposes a portion of said second surface of said stiffener.

11. The package of claim 10, wherein said at least one opening is formed to allow at least one wire bond to couple an IC die to said exposed portion through said at least one opening.

12. The package of claim 10, wherein said at least one opening is formed to allow at least one wire bond to couple at least one trace on a second surface of said second substrate to said exposed portion through said at least one opening.

13. The package of claim 1, wherein said second substrate has an edge formed to expose a portion of said second surface of said stiffener.

14. The package of claim 13, wherein said edge is formed to allow at least one wire bond to couple an IC die to said exposed portion.

15. The package of claim 13, wherein said edge is formed to allow at least one wire bond to couple at least one trace on a second surface of said second substrate to said exposed portion.

16. The package of claim 1, wherein said second substrate has a first opening, wherein said stiffener has a second opening that substantially coincides with said first opening to expose a portion of said surface of said first substrate.

17. The package of claim 16, wherein said first opening and said second opening are formed to allow at least one wire bond to couple an IC die to said exposed portion through said first opening and said second opening.

18. The package of claim 16, wherein said first opening and said second opening are formed to allow at least one wire bond to couple at least one trace on a second surface of said second substrate to said exposed portion through said first opening and said second opening.

19. The package of claim 16, wherein said second substrate is formed to expose a portion of said second surface of said stiffener, wherein said first opening and said second opening are formed to allow at least one wire bond to couple said exposed portion of said second surface of said stiffener to said exposed portion of said surface of said first substrate through said first opening and said second opening.

20. The package of claim 3, further comprising:

an IC die attached to said second surface of said stiffener through said centrally located opening.

21. The package of claim 20, wherein said second substrate is formed to expose a portion of the second surface of said stiffener, said package further comprising:

at least one wire bond that couples said exposed portion to at least one of said IC die and a second surface of said second substrate.

22. The package of claim 20, wherein said stiffener and said second substrate are formed to expose a portion of said surface of said first substrate, said package further comprising:

at least one wire bond that couples said exposed portion of said surface of said first substrate to at least one of said IC die, said second surface of said stiffener, and a second surface of said second substrate.

23. The package of claim 20, further comprising:

at least one wire bond that couples said IC die to a second surface of said second substrate.

24. The package of claim 20, further comprising:

an electronic device mounted to a second surface of said second substrate.

25. The package of claim 24, wherein said electronic device is leaded or leadless.

26. The package of claim 24, wherein said electronic device is a passive or active component.

27. The package of claim 24, wherein said electronic device is a resistor, a capacitor, an inductor, or a second IC die.

28. The package of claim 1, wherein said first substrate has a second surface; and

wherein said second surface of said first substrate includes a plurality of solder ball pads.

29. The package of claim 28, further comprising:

a solder ball attached to each of said plurality of solder ball pads.

30. The package of claim 2, further comprising:

an IC die attached to said second surface of said second substrate in said central region;

an electronic device attached to said second surface of said second substrate.

31. The package of claim 1, wherein said IC package is a ball grid array package.

32. The package of claim 9, wherein a solder or silver-filled epoxy is used to couple the first surface of the thermal connector to said first surface of said stiffener

33. A method of assembling a ball grid array (BGA) package, comprising the steps of:

(a) attaching a surface of a first substrate to a first surface of a stiffener; and

(b) attaching a surface of a second substrate to a second surface of the stiffener.

34. The method of claim 33, further comprising the step of:

(c) mounting an IC die to a second surface of the second substrate.

35. The method of claim 33, further comprising the steps of:

(c) forming a centrally located opening in the second substrate; and

(d) mounting an IC die to the second surface of the stiffener through the centrally located opening.

36. The method of claim 33, further comprising the step of:

(c) forming at least one via through the first substrate.

37. The method of claim 36, wherein step (c) comprises the step of:

positioning the at least one via in a central region of the first substrate.

38. The method of claim 37, further comprising the steps of:

(d) forming a plurality of solder ball pads on a second surface of the first substrate; and

(e) coupling the stiffener to at least one of the plurality of solder ball pads with the at least one via.

39. The method of claim 38, wherein step (c) further comprises the step of:

forming a conductive material in the at least one via.

40. The method of claim 33, further comprising the steps of:

(c) forming a centrally located opening in the first substrate; and

(d) mounting a thermal connector to the first surface of the stiffener through the centrally located opening.

41. The method of claim 40, wherein step (d) includes the step of:

mounting the thermal connector to the first surface of the stiffener using a solder or silver-filled epoxy.

42. The method of claim 40, further comprising the step of:

(e) configuring a surface of the thermal connector to be coupled to a printed circuit board (PCB).

43. The method of claim 33, further comprising the step of:

(c) forming the second substrate to expose a portion of the second surface of the stiffener.

44. The method of claim 43, wherein step (c) comprises the step of:

forming at least one opening in the second substrate.

45. The method of claim 43, further comprising the step of:

(d) coupling at least one wire bond between an IC die and the exposed portion.

46. The method of claim 43, further comprising the step of:

(d) coupling at least one wire bond between at least one trace on a second surface of the second substrate and the exposed portion.

47. The method of claim 33, further comprising the steps of:

(c) forming a first opening in the second substrate; and

(d) forming a second opening in the stiffener that substantially coincides with the first opening to expose a portion of the surface of the first substrate.

48. The method of claim 47, further comprising the step of:

(e) coupling at least one wire bond between an IC die and the exposed portion.

49. The method of claim 47, further comprising the step of:

(e) coupling at least one wire bond between at least one trace on a second surface of the second substrate and the exposed portion.

50. The method of claim 47, further comprising the steps of:

(e) forming the second substrate to expose a portion of the second surface of the stiffener; and

(f) coupling at least one wire bond between the exposed portion of the second surface of the stiffener and the exposed portion of the surface of the first substrate.

51. The method of claim 34, further comprising the step of:

(d) coupling the IC die to the second surface of the second substrate with at least one wire bond.

52. The method of claim 34, further comprising the step of:

(d) mounting an electronic device to a second surface of the second substrate.

53. The method of claim 33, further comprising the steps of:

(c) forming an array of solder ball pads on a second surface of the first substrate; and

(d) attaching a solder ball to each of the solder ball pads.

54. The method of claim 33, wherein the IC package is a ball grid array package.

55. A method of making a plurality of integrated circuit (IC) packages, comprising the steps of:

(1) forming a stiffener strip that includes a plurality of stiffeners;

(2) forming a first substrate strip that includes a plurality of first substrates;

(3) forming a second substrate strip that includes a plurality of second substrates;

(4) laminating the first substrate strip to a first surface of the stiffener strip; and

(5) laminating the second substrate strip to a second surface of the stiffener strip, whereby a substrate/stiffener/substrate strip combination is created.

56. The method of claim 55, wherein step (1) includes the step of:

(a) panelizing a metal sheet into a plurality of metal strips that include the stiffener strip.

57. The method of claim 55, wherein step (1) includes the step of:

(a) forming at least one opening in each of the plurality of stiffeners in the stiffener strip.

58. The method of claim 57, wherein step (a) includes the step of:

using an acid etching process.

59. The method of claim 55, wherein step (1) includes the step of:

(a) plating at least one metal bond pad on the second surface of each of the plurality of stiffeners in the stiffener strip.

60. The method of claim 55, wherein step (1) includes the step of:

(a) depositing a metal onto a central region of the first surface of each of the plurality of stiffeners in the stiffener strip.

61. The method of claim 60, wherein step (a) includes the step of:

plating, coating, or forming the metal onto the central region of the first surface of each of the plurality of stiffeners in the stiffener strip.

62. The method of claim 61, further comprising the step of:

(6) mounting a thermal connector to the metal deposited central region of each of the plurality of stiffeners through a central opening in each of the plurality of first substrates.

63. The method of claim 62, wherein step (6) includes the step of:

mounting the thermal connector to the metal deposited central region of each of the plurality of stiffeners using a solder or silver-filled epoxy.

64. The method of claim 55, wherein step (2) comprises the step of:

(a) panelizing a tape sheet into a plurality of tape strips that include a first tape strip, wherein the first tape strip includes a plurality of tape sections.

65. The method of claim 64, wherein step (2) further comprises the step of:

(a) forming at least one via through each of the plurality of tape sections in the first tape strip.

66. The method of claim 65, wherein step (2) further comprises the step of:

(a) forming trace patterns on at least one surface of each of the plurality of tape sections in the first tape strip.

67. The method of claim 66, wherein step (2) further comprises the step of:

(a) solder masking the at least one surface of each of the plurality of tape sections in the first tape strip to expose at least one surface contact pad.

68. The method of claim 55, wherein step (2) comprises the step of:

(a) applying a laminate material to a surface of each of the plurality of first substrates in the first substrate strip.

69. The method of claim 55, wherein step (2) comprises the step of:

(a) forming a central opening in each of the plurality of first substrates in the second substrate strip.

70. The method of claim 69, further comprising the step of:

(6) mounting a thermal connector to the first surface of each of the plurality of stiffeners in the stiffener strip through the central opening in each of the plurality of first substrates.

71. The method of claim 55, wherein step (3) comprises the step of:

(a) panelizing a tape sheet into a plurality of tape strips that include a first tape strip, wherein the first tape strip includes a plurality of tape sections.

72. The method of claim 71, wherein step (3) further comprises the step of:

(a) forming at least one via through each of the plurality of tape sections in the first tape strip.

73. The method of claim 72, wherein step (3) further comprises the step of:

(a) forming trace patterns on at least one surface of each of the plurality of tape sections in the first tape strip.

74. The method of claim 73, wherein step (3) further comprises the step of:

(a) solder masking the at least one surface of each of the plurality of tape sections in the first tape strip to expose at least one surface contact pad.

75. The method of claim 55, wherein step (3) comprises the step of:

(a) applying a laminate material to a surface of each of the plurality of second substrates in the second substrate strip.

76. The method of claim 55, wherein step (3) comprises the step of:

(a) forming a central opening in each of the plurality of second substrates in the second substrate strip.

77. The method of claim 76, further comprising the step of:

(6) mounting an IC die to the second surface of each of the plurality of stiffeners in the stiffener strip through the central opening in each of the plurality of second substrates.

78. The method of claim 55, further comprising the step of:

(6) mounting an IC die to a surface of each of the plurality of second substrates in the second substrate strip.

79. The method of claim 78, further comprising the step of:

(7) attaching a wire bond between the IC die and a bond finger on the surface of each of the plurality of second substrates.

80. The method of claim 79, further comprising the step of:

(8) encapsulating the IC die on the surface of each of the plurality of second substrates.

81. The method of claim 55, further comprising the step of:

(6) singulating the substrate/stiffener/substrate strip combination into a plurality of separate substrate/stiffener/substrate combinations.

82. The method of claim 55, further comprising the step of:

(6) attaching a plurality of solder balls to a surface of each of the plurality of first substrates in the first substrate strip.